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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/901,280	07/09/2001	Giuseppe Rossi	08305-116001/20-31	7560

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Micron Technology Inc C/O Tom D'Amico
Dickstein, Shapiro, Moran & Oshinsky
2101 L Street NW
Washington, DC 20037-1526

EXAMINER
TRAN, NHAN T

ART UNIT	PAPER NUMBER
2615	9

DATE MAILED: 10/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/901,280	ROSSI ET AL.	
	Examiner	Art Unit	
	Nhan T. Tran	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Information Disclosure Statement

1. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 – 6, 10 – 11, 13 – 14 & 16 – 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Stark (US 2002/0179820).

Regarding claim 1, Stark discloses an apparatus comprising:

groups of image sensors (K clusters), each group comprising subgroup of sensors (504A-504D) (see Fig. 5);

subgroup select circuits (508A-508D), each of which coupled to an output from a respective subgroup of sensors (Fig. 5);

group select circuits (410 & 412 for selecting each column, i.e., 506), each of which is coupled to outputs from subgroup select circuits associated with a respective one of the groups (Figs. 4 & 5; page 5, [0078] & [0079]);

a bus (410, 412) coupled to outputs of the group select circuits (Fig. 4);

a controller for providing control signals to the subgroup select circuits and the group select circuits to selectively enable the respective subgroup select circuits and group select circuits to pass signals from the sensors to the bus one sensor at a time (Figs. 4 & 5; page 1, [0011] & [0012]; page 5, [0080] – [0082], wherein each charge is sequentially read out to the top/bottom sense amplifier 410/412 and to output buffer amplifier 416).

Regarding claim 2, the sensors are active pixel sensors (APS) as shown in page 1, [0008].

Regarding claim 3, a charge sensing circuit (amplifier) electrically coupled to the bus (see Figs. 4 & 5 for both sensing amplifier set and output buffer amplifier 416 are coupled to the bus).

Regarding claim 4, Stark shows that the number of group select circuit (e.g., 2 group select circuits, one for top select circuit of 410 and the other for bottom select circuit of 412) is

approximately equal to the square root of the number of subgroup select circuits (e.g., 4 subgroups 508A-508D) as shown in Figs. 4 & 5.

Regarding claims 5 & 6, Stark suggests that k clusters can be two or more (Fig. 5; page 5, [0078]. If k=16, then the ratio is 16:1).

Regarding claim 10, the claimed limitations "the controller is configured to provide the control signals to enable the switches in the group select circuits sequentially, and while a particular group select circuit switch is enabled, to enable the subgroup select circuits associated with the particular group select circuit sequentially, one at a time" are encompassed by the sequential readout of charges in the image sensor as analyzed in claim 1.

Regarding claim 11, the claimed limitations are analyzed with respect to claims 1 & 10.

Regarding claim 13, Stark discloses supergroups of sensors (e.g., upper and lower halves of image sensor as shown in Figs. 4 & 5);

inherent supergroup select circuits (at output of 410/412 or at input of 416), each of which is coupled to outputs from group select circuits associated with a respective one of the supergroups, wherein the controller is configured to provide control signals to the supergroup select circuits to selectively enable a supergroup select circuit to pass a signal from the bus to another bus (see Figs. 4 & 5). It is noted that the circuits shown in Fig. 4 inherently include

select circuits for selectively outputting charges from array 410 and 412 to the input of buffer amplifier 416 in order for the circuits to function properly in sequential readout.

Regarding claim 14, an output of each supergroup select circuit is coupled electrically to a common output bus (at 416 as shown in Fig. 4).

Regarding claim 19, Stark discloses a method comprising:

selectively enabling a supergroup select circuit (416) from an inherent set of supergroup select circuits (at output of 410/412 or at input of 416) and a series-connected group (column clusters connected in horizontal direction by 410/412 as shown in Figs. 4 & 5) select circuit from an associated set of group select circuits (i.e., column 506 includes an inherent select circuit for transferring charges from column 506 to top or bottom sense amplifier set) to electrically couple a charge mode read-out amplifier (i.e., a top/bottom sense amplifier set and output buffer amplifier 416) to a respective set of subgroup select circuits (508A-508D) (see page 5, [0078] & [0079]);

when the series-connected group select circuit and supergroup select circuit are so enabled, enabling a pixel output signal to pass from each subgroup select circuit of the respective set of subgroup select circuits in a sequential manner through the series-connected group select circuit and supergroup select circuit to the charge mode read-out amplifier (416); and disabling the group select circuit to electrically isolate the charge mode read-out amplifier from the respective set of subgroup select circuits (see Figs. 4 & 5; page 1, [0011] & [0012]; page 5, [0080] – [0082], wherein in order for charges to be sequentially read out to the top/bottom

horizontal transfer array 410/412 and to output buffer amplifier 416 properly, group select circuit of 410/412 and supergroup select circuit of 416 must be enabled and disabled accordingly and synchronously with sequential readout timing).

Regarding claim 20, the claimed limitations are analyzed with respect to claim 19 for repeating the same steps to sequentially read out all charges in the image sensor array.

Regarding claim 21, the claimed limitations are encompassed by the sequential readout of charges as analyzed in claims 19 & 20.

Regarding claims 22 & 23, the claimed limitations are also encompassed by the sequential readout of charges as analyzed in claims 19-21.

Regarding claim 16, the claimed limitations are encompassed by the analysis of claim 19.

Regarding claims 17 & 18, the claimed limitations are analyzed with respect to claims 20 & 21.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 7 – 9 & 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stark (US 2002/0179820).

Regarding claim 7, Stark teaches sequential readout of charges utilizing inherent switches for group selection as analyzed in claim 1, but Stark does not explicitly disclose each switch being a transistor switch with a respective gate terminal for receiving a control signal from the controller to enable (close) or disable (open) the switch. However, an Official Notice is taken that such a switch configured by a transistor by closing and opening its gate is well known in the art for sequentially reading charges output from a column to an opposed transfer array.

Therefore, it would have been obvious to one of ordinary skill in the art to recognize that each group select circuit in Stark comprises a transistor switch with respective gate terminal for receiving a control signal from the controller, wherein when the switch is turned on, the group select circuit is enabled to pass signals from associated subgroup select circuits to the bus, and when the switch is turned off, the group select circuit is disabled from passing signals from the associated subgroup select circuits to the bus.

Regarding claim 8, Stark discloses each subgroup select circuit comprises a transistor (i.e., 508A) with respective gate terminal for receiving a control signal from the controller, wherein when the subgroup select circuit is turned on, the subgroup select circuit is enabled to pass signals from an associated subgroup of sensors, and when the subgroup select circuit switch

is turned off, the subgroup select circuit is disabled from passing signals from the associated subgroup of sensors to the bus (see Fig. 5; page 5, [0080] & [0081]).

Regarding claim 9, the claimed limitations are encompassed by the sequential readout method in Stark as analyzed in claims 1, 7 & 8.

Regarding claim 15, the claimed limitations are similarly analyzed in claim 7 for supergroup select circuit comprises a transistor switch.

4. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stark (US 2002/0179820) in view of Decker et al (US 6,512,546).

Regarding claim 12, Stark does not explicitly disclose that each group select circuit comprises a pair of NMOS transistor switches. However, as taught by Decker, a group selection circuit in an image sensor can be implemented to provide multiple resolution output by utilizing a number of NMOS transistor switches, wherein full resolution readout is performed when a pair of NMOS transistors (CST1 & FT1, or CSB1 & FB1) are enabled for reading out charges to the top transfer bus or the bottom transfer bus, respectively (see Figs. 5 & 6; col. 9, lines 3-24).

Therefore, it would have been obvious to one of ordinary skill in the art to modify Stark with Decker to provide multiple resolution output of an image sensor by enabling NMOS transistor switches for selecting a full resolution when a pair of NMOS switches is enabled.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (703) 605-4246. The examiner can normally be reached on Monday - Thursday, 8:00am - 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew B Christensen can be reached on (703) 308-9644. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

NT.

ANDREW CHRISTENSEN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600